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EXAMINER	
ALMO, KHAREEM E	

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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,799	LORENZ, PERRY SCOTT	
	Examiner	Art Unit	
	KHAREEM E. ALMO	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/5/2008 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1-3, 5-11, 13-24 and 26-30 rejected under 35 U.S.C. 102(b) as being anticipated by Azimi et al. (US 6163183).

With respect to claim 1, figure 3 of Azimi et al. (US 6163183) discloses a circuit for temperature sensing, comprising: a comparator circuit (20) that is arranged to provide a trigger signal by comparing a reference signal (25) to a temperature sensor signal (24); a gate circuit (10) that is arranged to provide an output signal (100) by gating a gate input signal (12) subject to control by a gate Control signal, wherein the gate input signal is based at least in part on the trigger signal, and wherein the gate

control signal is based at least in part on a power-on-reset signal (120); and a hysteresis-and-output-sensor circuit (32 and 34) that is configured to control the reference signal in response to a sensed signal, wherein the sensed signal is based at least in part on the output signal.

With respect to claim 2, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the power-on-reset (120) signal is the gate control signal.

With respect to claim 3, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, further comprising: a timer circuit (36 and 38) that is configured to provide a mute signal in response to the power-on-reset signal (120), wherein the mute signal is the gate control signal.

With respect to claim 5, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the sensed signal is the output signal (100), and wherein the gate input signal is the trigger signal (12).

With respect to claim 6, figure 3 of Azimi et al. (US 6163183) the circuit of Claim 1, wherein the gate circuit is configured to provide the output signal such that a logic level of the output signal (100) corresponds to a logic level of the trigger signal (12) if the gate control signal corresponds to an inactive level, and the logical level of the output signal (100) corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 7, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, wherein the gate circuit includes an AND gate (10).

With respect to claim 8, figure 3 of Azimi et al. (US 6163183) discloses the circuit

of Claim 1, wherein the comparator circuit (20) is configured to provide the trigger signal such that the trigger signal corresponds to a first logic level if a voltage associated with the reference signal is greater than a voltage associated with the temperature sensor signal (22), and the trigger corresponds to a second logic level if the voltage associated with the reference signal is less than the temperature sensor signal (22).

With respect to claim 9, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 1, further comprising: a reference circuit (producing Vmonitor) that is configured to provide the reference signal in conjunction with the hysteresis-and-output-sensor circuit (32 and 34), wherein the hysteresis-and-output-sensor circuit is arranged to modify the reference signal if the hysteresis-and-output-sensor circuit is enabled, and wherein the hysteresis-and-output-sensor circuit is disabled if the output signal corresponds to a first logic level.

With respect to claim 10, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 9, wherein the reference circuit includes: a resistor (30) that is coupled to the hysteresis-and-output-sensor circuit (32 and 34) and the comparator circuit (20); and a current source circuit (38) that is configured to provide a current to the resistor.

With respect to claim 11, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 10, wherein the hysteresis-and-output-sensor circuit (32 and 34) is configured to provide a hysteresis current to the resistor (30) if the output signal corresponds to the second logic level.

With respect to claim 13, figure 3 of Azimi et al. (US 6163183) discloses a method for temperature sensing, comprising: activating hysteresis (via 34) if a

temperature-sensing condition has occurred; and ensuring that the hysteresis is automatically inactive (via 38 or 120) when the circuit is powering up.

With respect to claim 14, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 13, further comprising providing a reference signal (25), wherein activating the hysteresis includes modifying the reference signal (via 34), and wherein the hysteresis is active if the output signal corresponds to a first logic level.

With respect to claim 15, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 13, wherein ensuring includes providing an output signal (100) in response to a gate input signal (12) and a gate control signal (14), wherein the gate control signal is derived form a power-on-reset signal (120), a logic level of the output signal (16) corresponds to a logic level of the gate input signal (12) if the gate control signal corresponds to an inactive level, and the logical level of the output signal corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 16, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 15, furthering comprising: comparing a temperature sensor signal (24) to a reference signal (25); and providing a trigger signal in response to the comparison, wherein the gate input signal (12) is based at least in part on the trigger signal.

With respect to claim 17, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 15, wherein providing the output signal includes performing a logical AND function (10) on the gate input signal (12) and the gate control signal (14).

With respect to claim 18, figure 3 of Azimi et al. (US 6163183) discloses the method of Claim 15, further comprising: applying a power supply signal; and providing

the gate control signal in response to the power-on-reset signal (120), wherein providing the gate control signal (12) includes: providing the gate control signal such that the gate control signal corresponds to an active logic level when the power supply signal is initially applied, and for a pre-determined period of time thereafter; and

providing the gate control signal such that the gate control signal corresponds to an inactive level after the pre-determined period of time.

With respect to claim 19, figure 1 of Azimi et al. (US 6163183) discloses the method of Claim 15, further comprising: providing a first current; and converting a reference current into the reference signal (25), wherein activating the hysteresis includes: providing a hysteresis current if the output signal corresponds to a first logic level; providing substantially no current if the output signal corresponds to a second logic level; and providing the reference current by combining the first current and the hysteresis current.

With respect to claim 20, figure 3 of Azimi et al. (US 6163183) discloses a circuit for temperature sensing, comprising: means for activating hysteresis (32, 34 and 38) if a temperature-sensing condition has occurred; and means for ensuring that the hysteresis is automatically inactive when the circuit is powering up (input from 120).

With respect to claim 21, figure 3 of Azimi et al. (US 6163183) discloses the circuit of claim 1, wherein the circuit for temperature sensing is arranged such that the comparator circuit (20) trips when the temperature sensed by the temperature sensor signal (24) reaches a predetermined level (based on the reference signal 25).

With respect to claim 22, figure 3 of Azimi et al. (US 6163183) discloses the circuit of claim 1, wherein the temperature sensor signal (24) is indicative of a temperature (via thermal expansion).

With respect to claim 23, figure 3 of Azimi et al. (US 6163183) discloses the circuit of claim 1, wherein the temperature sensor signal (24) is proportional to a temperature.

With respect to claim 24, figure 3 of Azimi et al. (US 6163183) discloses wherein the comparator circuit (20) compares the temperature sensor signal (24) to the reference signal (25) in order to perform a temperature comparison.

With respect to claim 26 and 28-30, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. (See Ex parte Masham, 2 USPQ2d 1647 (1987).

With respect to claim 27, figure 3 of Azimi et al. (US 6163183) discloses the circuit of claim 13, wherein ensuring that the hysteresis is automatically inactive (during power failure) when the circuit is powering up is accomplished by disabling the hysteresis until the power up is complete (via comparator). (see column 3 lines 55-62 and also see paragraph 3 lines 1-15, Note for a reset to occur the device must have been fully powered on and complete)

4. Claim 1-3, 5-11, 13-22, 24, 26 and 28-30 rejected under 35 U.S.C. 102(b) as being anticipated by Lim et la. (US 5614857)

With respect to claim 1, figure 4 of Lim et al. (US 5614857) discloses a circuit for temperature sensing, comprising: a comparator circuit (20) that is arranged to provide a trigger signal by comparing a reference signal (Vth) to a temperature sensor signal (Vin2); a gate circuit (AND45) that is arranged to provide an output signal (Vout2) by gating a gate input signal (input at AND45) subject to control by a gate Control signal, wherein the gate input signal is based at least in part on the trigger signal, and wherein the gate control signal is based at least in part on a power-on-reset signal (Vin1); and a hysteresis-and-output-sensor circuit (R41, R42 and Q41) that is configured to control the reference signal in response to a sensed signal, wherein the sensed signal is based at least in part on the output signal.

With respect to claim 2, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the power-on-reset (Vin1) signal is the gate control signal.

With respect to claim 3, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, further comprising: a timer circuit (30) that is configured to provide a mute signal in response to the power-on-reset signal (Vin1), wherein the mute signal is the gate control signal.

With respect to claim 5, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the sensed signal is the output signal (vout2), and wherein the gate input signal is the trigger signal.

With respect to claim 6, figure 4 of Lim et al. (US 5614857) the circuit of Claim 1, wherein the gate circuit is configured to provide the output signal such that a logic level of the output signal (Vout2) corresponds to a logic level of the trigger signal if the gate

control signal corresponds to an inactive level, and the logical level of the output signal (Vout2) corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 7, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the gate circuit includes an AND gate (AND45).

With respect to claim 8, figure 4 Lim et al. (US 5614857) discloses the circuit of Claim 1, wherein the comparator circuit (20) is configured to provide the trigger signal such that the trigger signal corresponds to a first logic level if a voltage associated with the reference signal is greater than a voltage associated with the temperature sensor signal (Vin2), and the trigger corresponds to a second logic level if the voltage associated with the reference signal is less than the temperature sensor signal (Vin2).

With respect to claim 9, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 1, further comprising: a reference circuit (R45 and Q45) that is configured to provide the reference signal in conjunction with the hysteresis-and-output-sensor circuit (R41, R42 and Q41), wherein the hysteresis-and-output-sensor circuit is arranged to modify the reference signal if the hysteresis-and-output-sensor circuit is enabled, and wherein the hysteresis-and-output-sensor circuit is disabled if the output signal corresponds to a first logic level.

With respect to claim 10, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 9, wherein the reference circuit includes: a resistor (R45) that is coupled to the hysteresis-and-output-sensor circuit (R41, R42 and Q41) and the comparator circuit (20); and a current source circuit (Q45) that is configured to provide a current to the

resistor.

With respect to claim 11, figure 4 of Lim et al. (US 5614857) discloses the circuit of Claim 10, wherein the hysteresis-and-output-sensor circuit (R41, R42 and Q41) is configured to provide a hysteresis current to the resistor (R45) if the output signal corresponds to the second logic level.

With respect to claim 13, figure 4 of Lim et al. (US 5614857) discloses a method for temperature sensing, comprising: activating hysteresis (via Q41) if a temperature-sensing condition has occurred; and ensuring that the hysteresis is automatically inactive (via 30) when the circuit is powering up.

With respect to claim 14, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 13, further comprising providing a reference signal (Vth), wherein activating the hysteresis includes modifying the reference signal (via Q41), and wherein the hysteresis is active if the output signal corresponds to a first logic level.

With respect to claim 15, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 13, wherein ensuring includes providing an output signal (Vout2) in response to a gate input signal (Vout2) and a gate control signal (Vout1), wherein the gate control signal is derived form a power-on-reset signal (Vin1), a logic level of the output signal (Vout2) corresponds to a logic level of the gate input signal (Vout2) if the gate control signal corresponds to an inactive level, and the logical level of the output signal corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 16, figure 4 of Lim et al. (US 5614857) discloses the

method of Claim 15, furthering comprising: comparing a temperature sensor signal (Vin2) to a reference signal (Vth); and providing a trigger signal in response to the comparison, wherein the gate input signal is based at least in part on the trigger signal.

With respect to claim 17, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, wherein providing the output signal includes performing a logical AND function (AND45) on the gate input signal (Vout2) and the gate control signal (Vout1).

With respect to claim 18, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, further comprising: applying a power supply signal; and providing the gate control signal in response to the power-on-reset signal (Vin1), wherein providing the gate control signal (Vout1) includes: providing the gate control signal such that the gate control signal corresponds to an active logic level when the power supply signal is initially applied, and for a pre-determined period of time thereafter; and providing the gate control signal such that the gate control signal corresponds to an inactive level after the pre-determined period of time.

With respect to claim 19, figure 4 of Lim et al. (US 5614857) discloses the method of Claim 15, further comprising: providing a first current (through Q45); and converting a reference current into the reference signal (Vth), wherein activating the hysteresis includes: providing a hysteresis current if the output signal corresponds to a first logic level; providing substantially no current if the output signal corresponds to a second logic level; and providing the reference current by combining the first current and the hysteresis current.

With respect to claim 20, figure 4 of Lim et al. (US 5614857) discloses a circuit for temperature sensing, comprising: means for activating hysteresis (Q41) if a temperature-sensing condition has occurred; and means for ensuring that the hysteresis is automatically inactive when the circuit is powering up (input from Vin).

With respect to claim 21, figure 4 of Lim et al. (US 5614857) discloses the circuit of claim 1, wherein the circuit for temperature sensing is arranged such that the comparator circuit (20) trips when the temperature sensed by the temperature sensor signal (Vin2) reaches a predetermined level (based on the reference signal Vth).

With respect to claim 22, figure 4 of Lim et al. (US 5614857) discloses the circuit of claim 1, wherein the temperature sensor signal (Vin2) is indicative of a temperature.

With respect to claim 24, figure 4 of Lim et al. (US 5614857) discloses wherein the comparator circuit (20) compares the temperature sensor signal (Vin2) to the reference signal (Vth) in order to perform a temperature comparison.

With respect to claim 26 and 28-30 it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. (See Ex parte Masham, 2 USPQ2d 1647 (1987).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azimi et al. (US 6163183) in view of Nakajima et al. (US 6417704).

With respect to claim 4, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 3, but fails to disclose the detail of circuit that generates the reset signal. However, Nakajjima et al.'s figure 1 shows a reset signal generation circuit in response to the circuit power supply and having low power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Nakajima et al.'s reset circuit to generate Azimi et al.'s reset signal for the purpose of saving power consumption. It is further noted that it is seen as an obvious design preference to select Nakajima et al.'s output signal or its complemented signal as the reset signal dependent on a particular environment of use to ensure optimum performance. Thus the modified Azimi et al.'s circuit further shows that the timer circuit includes a one-shot timer circuit (Nakajima et al.'s 12), wherein the one-shot timer circuit is configured to provide the mute signal such that the gate control signal such that the mute signal corresponds to an active logic level when a power supply signal is applied to the circuit, and for a pre-determined period of time thereafter; and such that the mute signal corresponds to an inactive level after the pre- determined period of time.

With respect to claim 12, figure 3 of Azimi et al. (US 6163183) discloses the circuit of Claim 10, but fails to disclose wherein a resistance that is associated with the resistor (30) is adjustable. It is well know to use an adjustable resistor to optimize

resistance values in a circuit. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the resistor (30) in Azimi et al. with a variable resistor for the purpose of optimizing resistance.

With respect to claim 25, figure 3 of Azimi et al. discloses the circuit of claim 24 except for wherein the hysteresis and output sensor circuit is arranged to provide hysteresis in a range of about 2°C to about 10°C of hysteresis for the temperature comparison when the hysteresis is enabled. It would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange the hysteresis and output sensor circuit to provide hysteresis in the 2°C to about 10°C of hysteresis for the temperature comparison when the hysteresis is enabled, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves routine skill in the art. (See In re Aller, 105 USPQ 233.)

Response to Arguments

7. Applicant's arguments filed 12/20/2007 have been fully considered but they are not persuasive.

With respect to applicant's arguments that "Azimi fails to disclose , " a comparator circuit that is arranged to provide a trigger signal by comparing a reference signal to a temperature sensor signal", as recited in Applicant's claim 1, the Examiner disagrees. Applicant' goes on to further clarify that the signal at reference electrode 24 of FIG. 3 of Azimi is a bangap reference voltage, not a temperature sensor signal and that a bangap reference voltage is substantially independent of temperature and therefore cannot be

used as a temperature sensor signal. The examiner disagrees. Band gaps depend on temperature because of thermal expansion. Thermal expansion is the tendency of matter to change in volume in response to a change in temperature. The degree of expansion divided by the change in temperature is called the material's coefficient of thermal expansion and generally varies with temperature. As detailed on page 2 of the specification "the term "signal" means at least one current, voltage, charge, temperature, data, or other signal". In the Azimi reference, the signal is the voltage that is indicative of the temperature of the bandgap. Although the Applicant cites Brokaw to refute a bandgap voltage being dependent of temperature, the Applicant admits it is only substantially independent of temperature and therefore dependent on temperature. Furthermore Brokaw states this case in which the PTAT and CTAT are combined are only when the choice of certain parameters are distinctively and precisely chosen. These parameters are based on are based a specific circuit in the Brokaw reference which have PTAT dependent on the base to emitter connections of a first transistor and CTAT dependent on the base to emitter connections of a second transitor which are positioned at the input of the operational amplifier which produces the band gap, (with markedly different current densities). However this circuit arrangement is not used in Azimi and therefore does not have a bearing on the independence of the temperature. Therefore the circuit in Azimi does disclose wherein the bandgap reference voltage is dependent on temperature.

With respect to applicant's argument that Azimi fails to disclose, "activating hysteresis if a temperature sensing condition has occurred", the Examiner disagrees.

Because, the bandgap voltage sensed via the comparator also senses the a temperature condition and the hysteresis is activated based on that condition via feedback loop through 10 and 34, the condition is also met.

With respect to applicant's argument that Azimi fails to disclose "comparing a temperature sensor signal to a reference signal", because the signal at 24 is a temperature sensor signal as discussed above in regard to claim 1, the rejection is maintained.

With respect to applicant's argument concerning claim 25, that Azimi does not teach wherein the hysteresis and output sensor circuit is arranged to provide hysteresis in a range of about 2 to 10 degrees C for the temperature comparison is enabled. The Examiner contends that the the general conditions are disclosed because the inputs of the comparator can be interpreted as temperature signals and therefore temperatature comparison is performed. Furthermore, depending on the wire and the resistance the temperature would operate in the aforementioned range.

With respect to applicant's argument that Azimi fails to disclose "means for activating hysteresis if temperature-sensing condition has occurred", the examiner disagrees. Circuits 32, 34 and 38, are the means that activate hysteresis via the closing of 38 if the function of a temperature sensing condition from 24 has occurred. As such Azimi reads on the claim.

With respect to applicant's argument against Lim, the Examiner disagrees. If a voltage changes it is inherent the temperature changes because resistance changes. However small the temperature change is it is still inherent in the circuit that

temperature changes. Whether an increase or decrease is only a slight change is detectable.

With regard to applicant's argument that resistance that if the current through a resistor increases, it is the increase in current that causes the voltage to increase not temperature, the Examiner agrees, however the temperature of resistor R11 increases as the current thought it increases because the resistance is dependent on resistivity which is dependent on temperature.

With respect to applicant's argument that Lim fails to disclose, " a gate circuit that is arranged to provide an output signal by gating a gate input signal subject to control by a gate control signal, wherein the gate input signal is based at least in part on the trigger signal" as recited in claim 1, the Examiner disagrees. Applicant' argues that Vout2 is not provided by AND gate AND45 rather AND gate AND45 of FIG. 4 of Lim receives signal Vout1 and Vout2 as inputs, and provides a signal to the base of transistor Q45 as an output of AND gate AND45. According to Merriam Webster the definition of provide is "to supply or make available". Because the AND gate AND45 supplies the activation signal and/or the deactivation signal of Q45 which supplies the activation signal to OP20 to make Vout2 available, by a translation relationship AND45 makes Vout2 available, i.e provides for Vout2 and thus meets the claim language. Both the AND gates and the OP20 make Vout2 available.

With respect to applicant's argument that Lim fails to disclose "a comparator circuit that is arranged to provide a trigger signal by comparing a reference signal to a temperature signal", the Examiner disagrees. The temperature of resistor R11

increases as the current through it increase thereby providing a higher voltage Vin2. Since Vin2 is compared to Vth (a reference signal) the claim is met.

With respect to applicant's argument that Lim fails to disclose, wherein the gate control signal is based at least in part on a power-on-reset signal", the Examiner disagrees. In response to applicant's argument that voltage Vin1 of FIG. 4 of Lim is not a power on reset signal", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

With respect to applicant's arguments that Lim fails to disclose, "ensuring that the hysteresis is automatically inactive when the circuit is powering up" the Examiner disagrees. Unless the comparator 30, meets the predetermined threshold of 30, during power up the hysteresis is inactive, because no signal passes to the hysteresis circuit until the power up condition at 30 is met.

With respect to applicant's argument concerning Lim resistance always varies with temperature, that this statement is not true. The Examiner disagrees. The resistivity of an object always varies with temperature because there is a temperature coeffienct associated with resistivity. i.e. for silver the temperature coefficient is 4.1x10-3 with a resistivity of 1.62x10-8, for copper resistivity is 1.69x10-8 with a temperature coefficient of 4.3x10-3. Because the material's properties vary with temperature resistance always varies with temperature.

With respect to applicant's argument concerning the advisory action the Examiner disagrees. With respect to the Brokaw, Brokaw is in reference to a circuit with two transistors at the input of the Op amp and in respect to the change in the base to emitter voltage controlling the independence of the temperature. This is not the same as Azimi which has no transistors at the input of the op amp.

With respect to claim 21, any level is a predetermined level. So when the temperature sensed by the temperature sensor signal reaches any level, this reads on the claim. In Lim the comparator tripping at all reads on the claim because regardless when comparator trips there is an apparent level related to the tripping. The claim is not written in such a manner to evoke the meaning of a causal relationship but as a timing relationship.

With respect to Applicant's argument with respect to claim 24, the temperature sensor signal and the reference signal are compared in order to perform a temperature comparison is interpreted merely tom mean that the temperature sensor signal and the reference signal have some component indicative of a representation of temperature. In the Lim prior art resistance is indicative of a temperature, the higher the resistance the more heat given off and the more temperature present.

With respect to TC being a zero temperature coefficient the change in Vin1 is based on the temperature coefficient being zero and therefore is still based on temperature.

With respect to applicant's argument concerning when or before, the Examiner has interpreted when to include before powering up because powering up is a process that includes before the signal is powered up.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khareem E Almo/
Examiner, Art Unit 2816

/QUAN TRA/
Primary Examiner, Art Unit 2816